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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,113	BEAUJOIN ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 9-31 have been examined.

Drawings

2. The examiner would like to point out that method claims are typically illustrated by a simple flowchart(s) with the boxes containing the steps of the method. These drawings aid in the understanding of the claimed invention.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 9, 11, 14-17, 20-23, 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US-6108802), hereinafter Kim, in view of Martens (US-5751727), hereinafter Martens.

Claims 9, 11, 14, 20 and 26:

Kim teaches a dual-port RAM-type FIFO memory device 100 (hereinafter referred to as the FIFO 100) comprised of a Random Access Memory (RAM) 102 that has n storage rows or words (shown in FIG. 3) where the input port 104 of the RAM 102 is connected to a Data Input Register (DIR) 108 and the output port 106 of the RAM 102 is connected to a Data Output Register (DOR) 110. Kim also teaches the FIFO 100 further includes a Write Address Register (WAR) 112 and a Read Address Register (RAR) 114 where each register 112 and 114 is M-bits wide, where M is an integer equal to the number of bits needed to address a RAM containing n words (a sequential access memory array storing p words each of n bits). (Col. 4, lines 34-50). Kim further teaches that BIST capability is provided by a BIST control 122 that controls a Test Pattern Generator (TPG) 118, which generates test patterns in the form of vectors for input to the RAM 102, and a Output Data Evaluator (ODE) 120. In addition, Kim teaches during testing intervals, multiplexer 121 passes test patterns from the TPG 118 to the DIR 108 for input to the RAM 102 (writing the memory array). Kim discloses that the ODE 120 is coupled to the output of the DOR 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data) and acts to compact or otherwise optimize the data output from the DO line during test intervals based on responses generated by the RAM 102 to the test patterns provided by the TPG 118 (comparing the test bits of the extracted test words with expected data bits). (Col. 6, lines 23-49). Kim does not explicitly teach the test words are "sequentially" extracted or compared. However, Kim does teach the Output Data Evaluator (ODE) 120 is coupled to the output of the Data Output Register (DOR) 110 so as to receive the

same data that is output to the Data Output (DO) line (extracting the p words from the data). Martens teaches that it is necessary to have the capability to read data out of the array serially (sequentially extracting test words) in certain chip-testing conditions. Martens teaches this capability, which is referred to as "scan testing" the array, requires that the array be able to hold its results in a group of memory elements where these memory elements are connected in series such that the output from the first memory element is fed to the scan input of the second element. Martens also teaches the output of the last memory element is fed to a test circuit outside the array (Kim's Output Data Evaluator (ODE) 120) for comparison to some expectation value. (Col. 5, lines 13-55, Fig. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's Data Output Register (DOR) 110 with Martens' scan register configuration shown in Figure 4. The artisan would have been motivated to do so because it would enable Kim's Data Output Register (DOR) 110 to read data out of the array serially (sequentially extracting test words) and subsequently Kim's Output Data Evaluator (ODE) 120 will be able to compare the output test data sequentially before extracting the next test word.

Claims 15, 21,and 27:

Martens teaches latch output of column n is depicted at line 128 and scan output n-1 is read to scan input n as depicted at line 132. (Col. 5, lines 51-53, Fig. 4). The first and second control means disclose in the claimed invention is a typical capture (first control means) and shift (second control means) procedure which is commonly used in

the art and would be obvious to one skilled in the art. The comparator means is taught by Kim in the Output Data Evaluator (ODE) 120. (Col. 6, lines 23-49).

Claims 16, 22 and 28:

This claim is rejected per claims 14, 20 and 26 above. Also, Martens teaches that the array scan latch organization of FIG. 4 includes multiple scannable latch circuits that are coupled to one another. (Col. 6, lines 23-49).

Claims 17, 23 and 29:

Kim teaches that the ODE 120 is coupled to the output of the DOR 110 so as to receive the same data that is output to the Data Output (DO) line (extracting the p words from the data) and acts to compact or otherwise optimize the data output from the DO line during test intervals based on responses generated by the RAM 102 to the test patterns provided by the TPG 118 (comparing the test bits of the extracted test words with expected data bits). (Col. 6, lines 23-49). Kim does not explicitly disclose that the ODE 120 includes XOR and XNOR gates. However, Kim does teach the ODE 120 compacts or optimizes the data that is compared. It is well known in the art that this procedure is accomplished through a XOR or XNOR logic and, therefore, is inherent in Kim's ODE 120.

4. Claims 10, 12, 13, 18, 24, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US-6108802), hereinafter Kim, in view of Martens (US-5751727), hereinafter Martens, in further view of Zorian et al. (US-6330696), hereinafter Zorian.

Claims 10, 18, 24 and 30:

Kim does not explicitly teach the test words are written to obtain a checkerboard test pattern in the memory array. However, Kim does teach the RAM-type FIFO 100 may experience memory faults and functional faults associated with the RAM 102. (Col. 6, lines 66, 67, col. 7, line 1). Zorian teaches detection of junction leakage faults is accomplished by storing a pattern of alternating values in neighboring cells, such as storing a "checkerboard" pattern of"1"s and "0"s in the memory array. (Col. 4, lines 59-62, col. 6, lines 37-40, 46-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's fault detection algorithm to include Zorian's algorithm to detect junction leakage faults by writing a checkerboard pattern to the memory array. The artisan would have been motivated to do so because it would increase quality of the memory array test. Kim teaches that BIST capability is provided by a BIST control 122 that controls a Test Pattern Generator (TPG) 118, which generates test patterns in the form of vectors for input to the RAM 102 (obtaining the expected data bits). (Col. 6, lines 23-36).

Claim 12:

Kim does not explicitly teach the test words are written to obtain a checkerboard test pattern in the memory array. However, Kim does teach the RAM-type FIFO 100 may experience memory faults and functional faults associated with the RAM 102. (Col. 6, lines 66, 67, col. 7, line 1). Zorian teaches detection of junction leakage faults is accomplished by storing a pattern of alternating values in neighboring cells, such as storing a "checkerboard" pattern of"1"s and "0"s in the memory array. (Col. 4, lines 59-

62, col. 6, lines 37-40, 46-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's fault detection algorithm to include Zorian's algorithm to detect junction leakage faults by writing a checkerboard pattern to the memory array. The artisan would have been motivated to do so because it would increase quality of the memory array test.

Claim 13:

Kim teaches that BIST capability is provided by a BIST control 122 that controls a Test Pattern Generator (TPG) 118, which generates test patterns in the form of vectors for input to the RAM 102 (obtaining the expected data bits). (Col. 6, lines 23-36).

5. Claims 19, 24, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US-6108802), hereinafter Kim, in view of Martens (US-5751727), hereinafter Martens, in further view of Zorian et al. (US-6330696), hereinafter Zorian, and in even further view of Biskup et al. (US-6751757), hereinafter Biskup.

Claims 19, 24, and 31:

Kim does not explicitly teach **"the generator means comprises: first delivery means for generating a least significant bit of each read address; a counter for storing a binary word representative of the rank of a test bit in the current test word extracted from the memory array; second delivery means for generating a least significant bit of each binary word in the counter; and one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate comprising two inputs connected to respective outputs of the first and second delivery means, and an output**

sequentially delivering the expected data bits." However, Kim does teach that BIST capability is provided by a BIST control 122 that controls a Test Pattern Generator (TPG) 118, which generates test patterns in the form of vectors for input to the RAM 102 (obtaining the expected data bits). (Col. 6, lines 23-36). Biskup teaches a set of XOR gates 730 implements the one's complement by inverting the CRC data from the CRC generation circuit 716 (first delivery means) and the LBA data from an LBA generation circuit 732 in response to the least significant bit (LSB) of an address of a word counter 734 (counter and second delivery means). Biskup also teaches the word counter 734 increments in response to each 16-bit word count, and in the illustrated embodiment, the LSB of the word counter 734 inverts every other word by asserting a logic "1" state as an input to the set of XOR gates 730 (one of an EXCLUSIVE OR and EXCLUSIVE NOR logic gate). (Col. 11, lines 24-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kim's BIST control 122 and Test Pattern Generator (TPG) 118 to incorporate Biskup's CRC generation circuit 716 (first delivery means), word counter 734 (counter and second delivery means) and XOR gates 730. The artisan would have been motivated to do so because this would enable Kim to generate a simplified expected data based on the checkerboard test pattern for fault testing purposes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

SUPERVISORY PATENT EXAMINER
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